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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/632,067	07/31/2003	Gerard Chauvel	TI-35423 (1962-05402)	2049

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EXAMINER	
GU, SHAWN X	

ART UNIT	PAPER NUMBER
2189	

DATE MAILED: 04/25/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/632,067	CHAUVEL ET AL.	
	Examiner	Art Unit	
	Shawn Gu	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 March 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,6,7,9,11,14-20 and 22* is/are rejected.

7)☒ Claim(s) *2,4,5,8,10,12,13,21,23* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This final Office action is in response to the amendment filed 3 March 2006. Claims 1-23 are pending. All objections and rejections not repeated below are withdrawn.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 6, 7 and 14 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As for claims 6 and 14, the Examiner is unclear compared to what entity in the claimed invention does the data memory have a higher priority during hit/miss determination.

As for claim 7, the claim recites the limitation "the 2-way set associative cache". There is insufficient antecedent basis for this limitation in the claim.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1, 3, 7, 9, 11, 15-20 and 22 are rejected under U.S.C. 102(b) as being anticipated by Tremblay et al. [6,125,439].

As for claims 1, 9, 17 and 20, Tremblay et al. discloses a processor (Fig 1, 100), comprising:

a processing core that generates memory addresses to access a main memory (Fig 1, "To External Memory"; Fig 2; Col 7, Lines 30-31; Col 7, Lines 47-48) and on which a plurality of methods operate (Col 7, Lines 5-10), each method using its own set of local variables (Fig 4A; Fig 4B; Fig 4D); and

a cache subsystem comprising a multi-way set associative cache (Fig 1, 165; Col 20, Lines 54-59) and a data memory that holds a contiguous block of memory (Col 17, Lines 11-13; Fig 4A, Stack 400) defined by an address stored in a register (Col 8, Lines 10-20), wherein local variables are stored in said data memory (Col 8, Lines 50-60; Col 9, Lines 55-60).

The method of claim 20 is clearly performed by Tremblay et al.'s processor.

As for claims 3, 11 and 22, Tremblay et al. discloses that when a new method is called, the local variables associated with the called method use data memory space previously used by local variables associated with completed methods without generating a miss (Col 21, Lines 8-20).

As for claims 7 and 15, Tremblay et al. further discloses the processor of claim 1 wherein, if said data memory does not have sufficient capacity to store the local variables, then at least some local variables are stored in the multi-way set associative cache (Col 17, Lines 1-17; Col 19, Lines 61-65).

The cache subsystem of claim 15 is clearly comprised by Tremblay et al.'s processor.

As for claim 16, Tremblay et al. further discloses the cache subsystem of claim 15, wherein said local variables comprise local variables used in a stack-based instruction set (Col 7, Lines 16-20; Col 9, Lines 20-32).

As for claim 18, Tremblay et al. further discloses the cache subsystem of claim 17 includes a means for locking said local variables in said cache system (Col 20, Lines 54-62; Valid Bit is a means for locking).

As for claim 19, Tremblay et al. further discloses the cache subsystem of claim 17 includes a means for preventing said local variables from being written to external

memory upon completion of a method that uses said local variables (Col 20, Line 54-62; Valid Bit).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 6 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tremblay et al.

As for claims 6 and 14, Tremblay et al. discloses that request from data cache to external memory always has a higher priority than instruction cache request to external memory as a result of arbitration logic between internal and external components (Col 11, Lines 48-58). Although Tremblay et al. does not disclose granting higher priority to data memory containing the local variables during hit/miss determinations, it is obvious to one ordinarily skilled in the art at the time of the applicant's invention that since hit/miss determination might result in access to external memory, higher priority should be given to such data memory during that process, in order to allow the external

memory access arbitration logic of Tremblay et al. to grant a higher priority to data cache requests to external memory.

Allowable Subject Matter

8. Claims 2, 4, 5, 8, 10, 12, 13, 21 and 23 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

9. The Applicant failed to respond to the rejection of claim 7 in the first Office Action under 35 U.S.C 112, paragraph two. The rejection therefore stands.

Applicant's arguments filed on 3 March 2006 have been fully considered but they are not persuasive.

10. In the first argument (see Amendment, pg. 11, para.5, 6, pg 12, para.1-3), the Applicant argues that Tremblay does not teach or suggest "a data memory that holds a contiguous block of memory defined by an address stored in a register" and "the local variables are stored in said data memory".

However, in the first Office Action the Examiner already specifically argued that the Stack 400 in Fig 4A is a contiguous (a stack is always contiguous) block of data storage (memory). To make the argument more clear, it should be noted that the Stack 400 is contained in Stack Cache 155 (see Fig 4A and Fig 1, also col. 8, lines 47-52, "entries on stack 400 are contained on stack cache 155"), which is an array of registers implemented as a register file (see col. 7, lines 11-13), and the address space of this contiguous block of data memory that corresponds to Stack 400 is defined by a stack pointer stored in register OPTOP (see col. 8, lines 10-20, OPTOP points to top of Stack 400). A register file qualifies as a data memory as it stores (memorizes) data, and the portion of the register file (Stack Cache 155) that contains the Stack 400 is clearly a "data memory that holds a contiguous block of memory defined by an address stored in a register". Since it is already demonstrated that the stack 400 is contained in Stack Cache 155, it should therefore be clear that "the local variables are stored in said data memory" (see Fig 4A, col. 8, lines 50-60, col. 9, lines 55-60, and also col.9, lines 55-61 which were cited by the Applicant).

11. In the second argument (see Amendment, pg. 16, para.4 to pg. 17, para.2), the Applicant argues that the cited reference in Tremblay "has to do with determining priority between two internal components – data cache controller 161 and instruction cache controller 121) and the conclusion of obviousness is result of hindsight.

In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that

any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

The conclusion of obviousness made by the Examiner in claims 6 and 14 is based on the fact that during hit/miss determination of local variables in a cache memory (stack cache 155 and data cache 165), a miss would result in a read access to external memory (External Memory, not shown but suggested by Fig 1). Cache miss handling is a well-known teaching in the art at the time of the Applicant's invention and therefore is not considered hindsight reconstruction. Tremblay further teaches that its arbitration logic gives a higher priority to data cache than instruction cache when both are requesting access to external components (see col. 11, lines 48-58), and the cache that contains local variables is also a data cache that might request access to external memory when a miss occurs.

Furthermore, claims 6 and 14 did not clarify between what components is the priority determined. Therefore it is irrelevant if Tremblay's components are internal or external. It is also already made clear by Tremblay that the priority is used to determine order of access to external memory by internal components (data cache and instruction cache)

As a result, Tremblay teaches the limitations of claims 6 and 14 as already presented in above and also in the first Office Action.

12. Applicant's amendment necessitated the new rejection of Claims 6 and 14 under 35 U.S.C 112, second paragraph. Otherwise, no new ground of rejection is presented. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a). A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shawn Gu whose telephone number is (571) 272-0703. The examiner can normally be reached on 9am-5pm, Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Reginald Bragdon can be reached on (571) 272-4204. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Shawn X Gu
Patent Examiner
Art Unit 2189

15 April 2006

Reginald G. Bragdon
REGINALD G. BRAGDON
PRIMARY EXAMINER